REMARKS

By the present amendment, the independent claims 1 and 7 are amended and claims 11-16 are cancelled without prejudice or disclaimer of the underlying subject matter thereof. These amendments are believed to place this application in condition for allowance at the time of the next Official Action, for the reasons discussed below.

Claims 1-16 as they previously appeared in the case were rejected under U.S.C. 112, first paragraph, as allegedly failing to comply with the written description requirement. Claims 1-16 were also rejected under U.S.C. 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicant has amended claims 1 and 7 (and cancelled claims 11-16) in a manner believed to overcome the rejection. Accordingly, the rejection of such claims and dependent claims on such claims is now moot.

Claims 1-16 were also rejected under 35 USC 103(a) as allegedly being unpatentable over RIVARD (PG Pub# US 2004/78508) in view of WEBER 5,596,708. That rejection is respectfully traversed.

The remaining independent claims 1 and 7 are amended to recite "a control unit which generates a check information on the basis of said data, transforms said data into a physical domain

of said cache memory so as to associate said data with physical addresses, thereafter stores newly written data corresponding to said physical addresses in a logical domain of said cache memory and **take precedence writing said data and check information over writing said newly written data to the disks"**.

With reference to the preferred embodiments illustrated in the specification, when data (first data) in the cache memory is going to be written to the disks ("YES" in S22 of Fig. 6), the first data and its check information are converted to physical domain (S25-S27 of Fig.6) and associated to the physical address. After that, any newly written data including "newly written data corresponding to the physical address" (second data) are stored in the logical domain of the cache memory (Fig. 5) and read and over-written in the physical domain ("YES" in S2 of Fig. 4, "YES" in S12 of Fig. 5).

However, the writing of the second data is delayed as long as the first data remains in the physical domain ("YES" in S24 of Figure 6). The first data is deleted from the physical domain when both of the first data and its check information are normally written to the disks ("NO" in S29 and S30 of Fig. 6, page 18, lines 3-6 and "NO" in S34 and S35 of Fig. 7). In other words, writing the first data and its check information takes precedence over writing of second data (page 12, lines 15-18). Thus, once a certain data and its check information are transformed into physical domain, <u>new data, that is to be written</u>

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to the same physical address of disks, is maintained in logical domain for being read and over- written and **is not written to the disks until the data and its check information is written to the disks**.   Due to this feature, for example, the same write processing as that before occurrence of a failure can be continuously executed to allow **data coherency to be maintained** (lines 5-7 of page 4).

By contrast, RIVARD is silent as to this feature. RIVARD only discloses that a read request to data already in the cache (Cached?=="Y") results in a fast return of data since the data is returned from the fast RAM memory rather than disk (paragraph 55), a content /lookup is used to determine if the incoming write command's block address matches any currently stored block addresses associated with currently cached data (paragraph 58) and, writes in a sequence that will result in maximum disk efficiency. For example, RIVARD may preferentially choose blocks from the Pending List that are nearby the current disk head position (paragraph 70).

Although RIVARD might imply that LBA (logical block address) is translated into a corresponding physical disk block location, usually in terms of cylinder-head-sector and preferentially choose blocks based on the physical address, it dose not mention anything about "take precedence writing said data and check information over writing said newly written data to the disks (corresponding to said physical address)".

Indeed, RIVARD makes no mention of "data to be newly written corresponding to said physical address", much less "take precedence writing said data and check information over writing said newly written data disks (corresponding to said physical address)".

WEBER also is silent about "a control unit which generates a check information on the basis of said data, transforms said data into a physical domain of said cache memory so as to associate said data with physical addresses, thereafter stores data to be newly written corresponding to said physical addresses in a logical domain of said cache memory and take precedence writing said data and check information over writing said newly written data to the disks". WEBER also does not mention "data to be newly written corresponding to said physical address", much less "take precedence writing said data and check information over writing said newly written data disks (corresponding to said physical address)".

As the above-mentioned feature is missing from each of the references, it is therefore also necessarily absent from the proposed combination and thus would not have been obvious to one having ordinal skill in the art.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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